REMARKS

Applicant appreciates the thorough examination of the present application that is reflected in the Official Action of October 28, 2004. In particular, Applicant appreciates the Examiner's careful review of the drawings and specification. In response, the specification and drawings have been amended as suggested by the Examiner. No new matter has been added. Accordingly, Applicant respectfully submits that pending Claims 1-12 are patentable for at least the reasons that now will be described.

The Drawing Objections Have Been Overcome

The drawings of the present application have been objected to under 37 C.F.R. 1.84(p)(5) as including reference characters not mentioned in the description. In particular, the Official Action asserts that the following reference characters are not mentioned in the description: OUTPUT DRIVER, PTRSTB, PTRST and 131 in Figure 1; all elements of Figure 2; 2nd STAGE, OUTPUT DRIVER, PTRSTB, PTRST, CLKDQ_F and CLKDQ_S in Figures 3 and 4; and all elements of Figure 5. *See* Official Action, Page 2. However, Applicant submits that many of the above-mentioned reference characters have been described in the specification as originally filed. For example, with reference to Figure 3 of the specification, "an output driver **331** of a memory device" is described. *See* Specification, Page 6, lines 29-34. Also, with reference to Figure 4, the specification describes "a second stage of an output multiplexing circuit...an output enable signal **PTRST**...[and] an inverted signal **PTRSTB**". *See* Specification, Page 8, lines 15-19. Further, at Page 7, the specification describes many of the elements of Figure 5, including signals CLK, DL0, DL1, CDQ0, CDQ1, QCLK0, QCLK1, QCLK2, QCLK3, and CLKDQ. *See* Specification, Page 7, lines 6-25. Nevertheless, for purposes of completeness, Applicant has amended the specification to include further descriptions of the above mentioned reference characters at page 2, line 28 to page 3, line 2; page 5, line 32 to page 6, line 5; page 6, lines 6-11; page 6, line 27 to page 7, line 5; page 7, lines 6-16; and page 7, lines 22-25. As these reference characters were included in the specification and drawings as originally filed, no new matter has been added.

The Official Action further objects to the drawings of the present application under 37 C.F.R. 1.83(a) as not showing every feature of the invention specified in the claims. In

particular, the Official Action asserts that the memory cell array, CAS latency information signal, clock signal, rising and falling edge of a delay signal of the clock signal, and output enable signal as recited by Claims 1-12 are not shown in the drawings. *See* Official Action, Pages 2-3. In response, Applicant has amended Figure 3 to include a memory cell array **330**. Attached hereto is a Replacement Figure 3. As the memory cell array was recited in the specification and claims as originally filed, no new matter has been added. However, Applicant submits that the CAS latency information signal, clock signal, rising and falling edges of a delay signal of the clock signal, and output enable signal as recited by Claims 1-12 are shown in the drawings as originally filed.

In particular, at Page 6, the specification describes "CAS latency information signals **CDQi** (i is an integer between 0 and n-1 inclusive)." *See* Specification, Page 6, lines 18-19. As such, where n=3, the CAS latency information signals include **CDQ0**, **CDQ1**, **CDQ2**, and **CDQ3**. Figures 3 and 4 illustrate that the second switch groups **321**, **322**, **333**, and **324** are activated responsive to signals **CDQ0**, **CDQ1**, **CDQ2**, and **CDQ3**, which, as defined at Page 6, are CAS latency information signals. Accordingly, the drawings illustrate CAS latency information signals as originally filed.

Likewise, at Page 6, the specification describes "a clock signal **CLK**" and "a rising edge **F** and a falling edge **S** of a delay signal **CLKDQ** of the clock signal **CLK**". *See* Specification, Page 6, lines 23 and 28-29. The timing diagram of Figure 5 illustrates this clock signal **CLK** as well as this delay signal **CLKDQ**. The rising and falling edges of the delay signal **CLKDQ** can also be seen in Figure 5 at the leading and trailing edges of each squarewave. As such, a clock signal and rising and falling edges of a delay signal of the clock signal are also illustrated in the drawings as originally filed.

Furthermore, at Page 8, the specification describes "an output enable signal **PTRST**" and "an inverted signal **PTRSTB** of the output enable signal **PTRST**". *See* Specification, Page 8, lines 17-19. As shown in Figure 3, output enable signal **PTRST** and inverted output enable signal **PTRSTB** are used to control output of the output driver **331**. Also, Figure 4 illustrates four NAND gates **ND1**, **ND2**, **ND3**, and **ND4** that are controlled in response to an output enable signal **PTRST**, and four NOR gates **NR1**, **NR2**, **NR3**, and **NR4** that are controlled in response to an inverted output enable signal **PTRSTB**. Thus, the drawings also illustrate an output enable signal as originally filed.

Accordingly, Applicant submits that the drawings are now in compliance with 37 C.F.R. 1.84(p)(5) and 1.83(a), and respectfully requests withdrawal of the outstanding objections.

The Section 112 Rejections Have Been Overcome

Claims 1-12 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Official Action states that the following reference characters shown in the drawings are not described in the specification: OUTPUT DRIVER, PTRSTB, PTRST and 131 in Figure 1; all elements of Figure 2; 2nd STAGE, OUTPUT DRIVER, PTRSTB, PTRST, CLKDQ_F and CLKDQ_S in Figures 3 and 4; and all elements of Figure 5. *See* Official Action, Page 4. As discussed above with reference to the drawing objections, many of the above mentioned reference characters are described in the specification as originally filed. Nevertheless, for completeness, Applicant has amended the specification to include further descriptions of the above mentioned reference characters. As these reference characters were included in the specification and drawings as originally filed, no new matter has been added.

The Official Action further asserts that some recitations of the claims are not understood because they are not shown in the drawings. In particular, the Official Action asserts that the memory cell array, CAS latency information signal, clock signal, rising and falling edge of a delay signal of the clock signal, and output enable signal as recited by Claims 1-12 are not shown in the drawings. *See* Official Action, Page 4. As discussed above with reference to the drawing objections, Applicant has amended Figure 3 to include a memory cell array **330**. However, as also discussed above, Applicant submits that the CAS latency information signal, clock signal, rising and falling edges of a delay signal of the clock signal, and output enable signal recited by Claims 1-12 are illustrated in the drawings as originally filed.

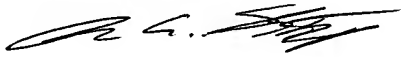
Moreover, the Official Action asserts that it is not understood how the circuits of Figures 3 and 4 are operating because all of the control signals of Figure 5 are not described in the specification. *See* Official Action, Pages 4-5. However, the specification as originally filed describes many of the signals shown in Figure 5, and has been amended to further describe these signals without adding new matter, as discussed above with reference to the

drawing objections. Accordingly, Applicant submits that Claims 1-12 are in compliance with the enablement requirement of 35 U.S.C. 112, first paragraph.

Conclusion

Applicant again appreciates the thorough examination of pending Claims 1-12. Applicant has now shown that all of the pending claims meet the statutory requirements for patentability. Accordingly, Applicant respectfully requests withdrawal of the outstanding objections and rejections and allowance of the present application.

Respectfully submitted,



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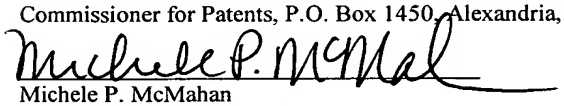

Michele P. McMahan
Date of Signature: January 28, 2005

Appendix A
Replacement Figures